EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S55	126	365/192.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/30 17:11
S61	984	713/500.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/31 12:39
S57	146	S54 and strobe	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/30 17:11
S58	39	S57 and FIFO	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/31 12:39
S59	1230	strobe same FIFO	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/30 17:17

	Document ID	Title	Inventor	Current OR
1	US 20060080566 A1	Low power clocking systems and methods	Sherburne; Robert Warren JR.	713/500
2	US 20050149774 A1	System and method for read synchronization of memory modules	Jeddeloh, Joseph M. et al.	713/500
3	US 6889334 B1	Multimode system for calibrating a data strobe delay for a memory read operation	Magro; James R. et al.	713/500
4	US 6085285 A	Intermixing different devices along a single data communication link by placing a strobe signal in a parity bit slot	Lucas; Gregg Steven et al.	711/112
5	US 20060061795 A1	Storage of key in arbitrary locations in memory	Walmsley; Simon Robert	358/1.14
6	US 20040193823 A1	Apparatus and method to switch a FIFO between strobe sources	Kelly, James D.	711/168
7	US 7016447 B1	Digital clock recovery PLL	Reuveni; David R.	375/371
8	US 5761464 A	Prefetching variable length data	Hopkins; Charles H.	710/310
9	US 20030226053 A1	Variably controlled delay line for read data capture timing window	Khieu, Cong Q. et al.	713/401
10	US 5768560 A	Dynamically configurable memory system having a programmable controller including a frequency multiplier to maintain memory timing resolution for different bus speeds	Lieberman; Donald A. et al.	711/167
11	US 5557751 A	Method and apparatus for serial data communications using FIFO buffers	Banman; David A. et al.	398/136